The ATLAS RPC ROD for Super LHC

A. Aloisio[a,b], L. Capasso[a,b], F. Cevenini[a,b], M. Della Pietra[b,c] R. Giordano[a,b] and V. Izzo[b]
[a] Università di Napoli "Federico II", Napoli, Italy [b] INFN – Sez. di Napoli, Italy [c] Università di Napoli "Parthenope", Napoli, Italy

Abstract

The number of interactions per bunch crossing for the upgrade of the Large Hadron Collider is expected to be ten times greater than the actual one. As a consequence, the ATLAS detector for SLHC foresees the use of a larger number of readout channels and also a new trigger level is under development. In order to face with such issue, we developed a new architecture for the Read Out Driver (ROD) for the ATLAS RPC Muon Spectrometer in the barrel region. Presently, each ROD board receives ATLAS RPC Muon readout data and arranges all the data fragments of a sector of the spectrometer in a unique event, sending it to the next acquisition systems. Our new design is based on the new generation Xilinx Virtex5 FPGA and it works with a clock frequency six times greater than the actual bunch crossing rate of the LHC. We also implemented the output channel of the ROD, presently based on S-Link protocol, by using the GTP transceivers inside the FPGA. We present an overview of our design, focusing on the newly added hardware features.

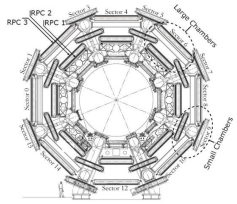

Fig. 1. ATLAS Barrel Muon Spectrometer in the azimuthal plane

Introduction

ATLAS is one of the four experiments built at the Large Hadron Collider (LHC) at CERN in Geneva, which is expected to start operations November 2009. ATLAS [1] is a general purpose detector aiming to find Higgs Boson and SUSY evidence. The ATLAS Muon Spectrometer has been designed and built to provide stand-alone trigger measurements and position measurements of muons. Its barrel section is made of Monitored Drift Tubes and Resistive Plate Chambers (RPCs) arranged in 32 sectors, to form two wheels surrounding the interaction point (Fig.1). The ATLAS Trigger and DAQ system has been designed on three levels. The First level trigger (L1) provides an initial reduction of a factor about 103 of the event rate, starting from the 40 MHz bunch crossing rate of the LHC, on the basis of information from the muon trigger chambers and calorimeters.

The First level trigger (L1) provides an initial reduction of a factor about 10^3 of the event rate, starting from the 40 MHz bunch crossing rate of the LHC, on the basis of information from the muon trigger chambers and calorimeters.
If the event is accepted by the L1 central trigger processor the Level 1 Accepted signal (L1A) is broadcasted. Data from the large number of detector readout channels are collected and packed into 1600 data fragments by the detector-specific *Read Out Driver* (RODs). From RODs, data are transferred optically to the next acquisition levels (ROSs), where data are temporarily stored and provided on request to the following stages of event selection.

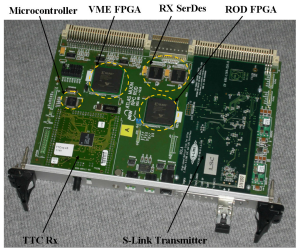

Fig. 2. Photo of the RPC ROD board

The RPC ROD board

The Muon RPC read-out data are transferred on optical link to the counting room and are received by the RX-SL boards. The RX/SL boards arrange Readout data in an event frame (RX Frame) and transmit them to the adjacent Read Out Driver across a custom backplane, via high speed serial links.
The RPC ROD [2] board (Fig.2) is based on two Xilinx Virtex-II FPGAs. The main task of the ROD is to perform a further framing of the readout data, together with a syntax analysis of the RX frames and a check of the coherence of Event Identifier numbers (EVID) casted in each RX frame. In order to store data and match different clock domains inside each FPGA, internal FIFOs have been used.
The dataflow of the Event Builder Engine is shown in Fig. 3. EVID data are stored in the EVID FIFO. Input data (coming from a specific RX/SL board) are stored in the corresponding FIFO (RX SerDes FIFO). Event builder output data are stored in the S-Link FIFO and then read out by the S-Link transmitter and sent across the optical link to the ROS.

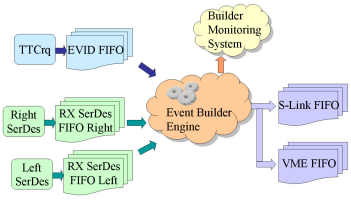

Fig.3. Dataflow of the ROD Event Builder Engine

ATLAS and the LHC Upgrade

The luminosity upgrade of the LHC is made of two main phases [2]. In the Phase 1 the proton injection system will be modified in order to obtain an expected luminosity of 3×10^{34} cm^{-2} s^{-1}, presumably in 2014. The Phase 2 foresees to reach a luminosity of 10×10^{34} cm^{-2} s^{-1} by 2019. The luminosity upgrade plans of the LHC will have considerable consequences on the ATLAS experiment, both on the detector side and on the trigger and DAQ systems.
The luminosity increase foreseen for the LHC upgrade leads to a corresponding increase in the mean number of interactions per bunch crossing, leading to a more intense particle production and a higher background. The main consequences of this increase in particle production is that the various detector are not able to sustain such an intense flux of particles. Thus, newer detectors have to be designed and developed, in order to manage the higher rate of particles. For the muon spectrometer, some R&D projects are under evaluation, that foresee the use of an additional RPC station. The main consequence of the use of these new detectors is the increase of readout channels, bandwidth and event size, that have to be managed by the DAQ system.
The trigger system has to be changed, in order to handle the huge amount of information coming from the detector and to correctly process the different requests of data validation. The present trigger upgrade plans focus on complicated trigger selection algorithms and pile-up handling. Probably, the three level trigger architecture will be changed in order accept or reject events with more accuracy.

The ROD board upgrade

Starting from the present upgrade plans on the ATLAS trigger and DAQ system, the present ROD architecture has some elements that can suffer from the request for a higher bandwidth and a higher data processing capability.
Fig. 4 shows (top) a simplified layout of the present ROD board. In the present ROD board design, the elements that could have potential problems, due to the high performance requests, are listed below:
1) The two SerDes channels
2) The S-Link output channel
3) The communication channel between VME and ROD FPGA
4) The Event Builder Frequency
5) The working frequency of the Internal FIFOs
The first three elements of the list are also labelled on fig.4 for clarity reasons.
For these reasons, we are currently re-designing the ROD board, giving a particular care to the architecture of *Event Builder Engine* inside the ROD FPGA and to the increased bandwidth requests, needed at the board's Input and Output.
The increasing requirements of high performance forced us to use the state-of-art FPGA technology. We performed a feasibility study, based on the evaluation of multiple implementations and simulations, using a XILINX VIRTEX 5 FPGA device as a benchmark. We propose a solution that could solve the bandwidth and data processing capability potential problems due to the ATLAS upgrade.
The main advantages in the use of a VIRTEX 5 device, in substitution of the VIRTEX II FPGA, are that the VIRTEX 5 offer a large amount of RAM blocks, a greater number of logic resources (~ 30000 vs. 10000 equivalent gates) and the Rocket I/O high speed serial links. Moreover, VIRTEX 5 has a dedicated logic in the RAM blocks that allows the user to easily implement high-speed FIFO modules (so-called Built-In FIFO); it also offers a network of high-speed clock trees, thus allowing to design a circuit architecture running at high clock frequency.
The new layout of the ROD board is shown in fig. 4 (bottom)

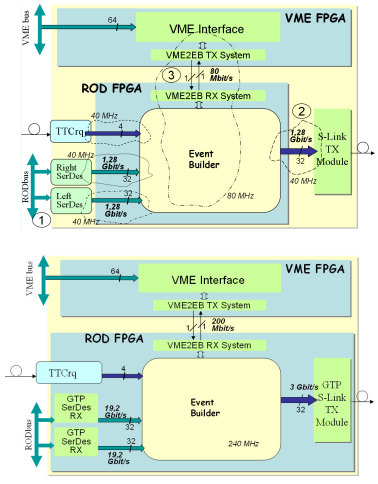

Fig. 4. The present (top) ROD board layout and the proposed new (bottom) board layout

Implementations and simulation

In the new layout of the ROD, the connections for the RODbus, the inter-FPGA communications and the S-Link module are based on GTP transceivers.
- As far as it concerns the RODbus, the present 8 lanes could be replaced by just 1 GTP-based serial connection running at 3 Gbps. By using the 8b/10b coding, the actual bandwidth for payload transmission will be 2.4 Gbps. Supposing to keep the same number of lanes on the new implementation, the new aggregate bandwidth will grow to 19.2 Gbps.
- The whole HOLA module will be replaced by logic implemented in the FPGA fabric encoding parallel data according the S-Link protocol. A GTP configured to work with 16-bit words and 8b/10b encoding will be used in place of the TLK2501 SerDes. Our S-Link emulator will be able to transmit serial data at a maximum data-rate of 3 Gbps and therefore will be potentially faster than the present S-Link module.
- The communication between the ROD FPGA and the VME FPGA can be implemented by means of a pair of GTP transceivers (one in each device). Each GTP encodes 16-bit incoming words clocked at 10 MHz according to the 8b/10b protocol and serialize them at 200 Mbps over a couple of differential pairs.
We performed an implementation optimized for design speed, resulting in the use of only the 18% of the logic resources. The timing analysis of the *Event Builder Engine* design shows that the working frequency can be pushed up to 240 MHz, three times the presently used frequency.

Conclusions

We presented a new design of the ATLAS Muon RPC ROD board, based on the new generation Xilinx Virtex5 FPGA, as a solution to the main potential bottlenecks foreseen for the ATLAS upgrade DAQ system. In particular, we performed a feasibility study, based on the evaluation of multiple implementations and simulations, using a XILINX VIRTEX 5 FPGA device as a benchmark. We present a comparison between the present ROD *Event Builder Engine* and the proposed one. The main benefits are due to the availability of the GTP Rocket I/O transceivers, to the use of new high performance FIFO modules and a network of high-speed clock trees. Our study shows that the state-of-art FPGA devices offer a considerable increase in data transfer bandwidth. The FPGA occupancy is lowered from 31% to 18%. The timing analysis tools show that the *Event Builder engine* on a new FPGA could work with a clock frequency six times greater than the actual bunch crossing rate of the LHC.

References

[1] ATLAS Collaboration, ATLAS Detector and Physics Performance - Technical Design Report - Volume I, May 1999
[3] M. Nessi, "The detector upgrade and upgrade scenarios", presented at the "ATLAS Upgrade "ROD" Workshop", CERN, Switzerland, June 2009

aloisio@na.infn.it, lcapasso@na.infn.it, cevenini@na.infn.it, delapietra@na.infn.it, rdo.dano@na.infn.it, izzo@na.infn.it